IN THE CLAIMS:

Please amend the claims as follows:

1. (Amended) An apparatus for communicated between a plurality of processor devices, comprising:

a post office memory including a plurality of mailbox memories;

each of the mailbox memories being write accessible at any time only by [its] a corresponding owner processor device, and read-accessible by [its] the corresponding owner processor device and other [the] processor devices of the plurality of processor devices at times determined independently of a write access.

2. (Amended) An apparatus as in claim 1, wherein:

the plurality of [processors] processor devices includes a transmitting processor device and a receiving processor device;

a signal line provides communication between the [processors] processor devices; and

a subroutine in the receiving processor device, corresponding to the signal line, reads [the] a mailbox memory [of] corresponding to the transmitting processor device.

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7. (Amended) An apparatus as in claim 5, wherein the plurality of [processors] processor devices comprises at least three processor devices, including at least two transmitting [processors] processor devices and at least one receiving processor device, and a signal line between the receiving processor device and each of the transmitting [processors] processor devices, further comprising:

(a) an OR gate producing a logical-OR of the signal lines; and

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(b) a mailbox status register associated with the receiving processor device, each of the signal lines setting a status of one of the transmitting [processors] processor devices in the mailbox status register.

8. (Amended) An apparatus as in claim 5, having at least three processor devices, including at least two transmitting [processors] processor devices and at least one receiving processor device, and a signal line between the receiving processor device and each of the transmitting [processors] processor devices, further comprising:

(a) an OR gate producing a logical-OR of the signal lines;

(b) a mailbox status register associated with the receiving processor device, each of the signal lines setting a status of one of the transmitting processors in the mailbox status register.

9. (Amended) An apparatus as in claim 1, wherein the post office memory is a multi-port random access memory (RAM), and each of the mailbox memories is a predetermined area of the RAM;

each predetermined area of the RAM further comprising means for providing write-access for only one of the processor devices to the predetermined area of the RAM from one [of the ports] port of the RAM; and

means for providing read-access to the RAM for the processor devices from each port of the RAM.

10. (Amended) An apparatus as in claim 9, wherein the [device is] multi-port RAM comprises a 4-port RAM.

11. (Amended) An apparatus as in claim 10, wherein [the] each predetermined area of RAM [is] comprises 8 bytes.

Claim 12, line 4, delete "post office" and insert --mailbox--;
line 15, after "the" insert --plurality of--;
line 17, delete "the" (first occurrence) and insert --a--.

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13. (Amended) A method of communicating among a plurality of processor devices, including a transmitting processor device and a receiving processor device, utilizing a post office with a plurality of mailboxes, the method comprising the steps of:

writing information into a predetermined one of the mailboxes in the post office [with] at any time determined a transmitting processor device;

signaling a receiving processor device with the transmitting processor device;

determining in the receiving processor device which of the processor devices signalled the receiving processor device; and

reading the information [in] from the predetermined mailbox with the receiving processor device at a time determined by the receiving processor.

Claim 14, line 2, after "processor" insert --device--.

Claim 15, line 3, after "processor" insert --device--.

Claim 16, line 2, after "processor" insert --device--;
line 3, after "processor" insert --device--.

Claim 17, line 1, delete "13" and insert --16--;
line 2, after "processor" insert --device--.

Claim 18, line 2, after "processor" insert --device--;
line 3, after "processor" insert --device--;
line 4, after "processor" insert --device--;

line 6, after "processor" insert --device--.

Claim 19, line 2, after "processor" insert --device--;
line 3, after "processor" insert --device--.

Claim 21, line 2, after "processor" insert --device--;
line 3, after "processor" insert --device--;
line 4, after "processor" insert --device--;
line 6, after "processor" insert --device--.

22. (Amended) A method of bi-directional communication between at least two processor devices, utilizing a post office RAM with a plurality of mailboxes, the method comprising the steps of:

writing information into a first mailbox in the post office RAM, and signaling a second processor device with a first processor device;

writing information into a second mailbox in the post office RAM, and signaling the first processor device with the second processor device;

determining in the second processor device which of the processor devices signalled [it] the second processor device;

determining in the first processor device which of the processor devices signalled [it] the first processor device;

reading the information in the first mailbox with the second processor device; and

reading the information in the second mailbox with the first processor device.

REMARKS

Claims 1-23 have been rejected under the second paragraph of 35 U.S.C. § 112 as being indefinite. The claims have been